

-40V P-Channel Enhancement Mode Power MOSFET

Product Summary

V_{DS}	$R_{DS(ON),MAX}$	I_{D_MAX}
-40 V	8.9 m Ω @ $V_{GS} = -10V$	-55 A
	14.8 m Ω @ $V_{GS} = -4.5V$	

Features

- P-Channel Enhancement Mode - Logic Level
- AEC-Q101 Qualified, PPAP Capable
- 175°C Operating Temperature
- 100% ΔV_{DS} & UIS & R_g Tested
- AEC-Q101 qualified (Automotive grade with suffix "Q".)
- Expsemi technology

Application

- General Automotive Applications

Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
EPT04P089LCFQ	PDFN3333-8L	P4008BLQ	13" Tape&Reel	5,000

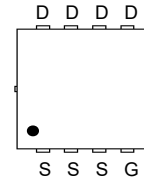
Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	-40	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = -10V$) ⁽¹⁾	I_D	$T_C = 25^\circ\text{C}$	-55
		$T_C = 100^\circ\text{C}$	-39
Pulsed Drain Current ⁽²⁾	I_{DM}	-222	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	212	mJ
Single Pulse Avalanche Current ($L = 0.1\text{mH}$)	I_{AS}	-35	A
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	45
		$T_C = 100^\circ\text{C}$	23
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +175	$^\circ\text{C}$

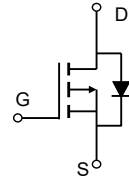
Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$	48	60	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$	2.5	3.3	$^\circ\text{C/W}$

PDFN3333-8L



PIN Configuration
(Top View)



Schematic Diagram

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$	-	-	-1.0	μA
			-	-	-100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1.2	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -20A$	-	7.2	8.9	m Ω
		$V_{GS} = -4.5V, I_D = -15A$	-	11.8	14.8	m Ω
Forward Transconductance	g_{fs}	$V_{DS} = -5.0V, I_D = -20A$	-	30	-	S
Diodes Forward Voltage	V_{SD}	$I_S = -2.0A, V_{GS} = 0V$	-	-0.7	-1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C_{iss}	$V_{DS} = -20V, V_{GS} = 0V, f = 1\text{MHz}$	-	1511	1964	pF
Output Capacitance	C_{oss}		-	1077	1400	pF
Reverse Transfer Capacitance	C_{rss}		-	70	140	pF
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$	-	12	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DS} = -20V$ $I_D = -20A, R_{GEN} = 3.0\Omega$	-	5.6	-	ns
Rise Time	t_r		-	13	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	47	-	ns
Fall Time	t_f		-	26	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge ($V_{GS} = -10V$)	Q_g	$V_{DS} = -20V, I_D = -20A$ $V_{GS} = -10V$	-	24	31	nC
Total Gate Charge ($V_{GS} = -4.5V$)	Q_g		-	11.8	15.3	nC
Gate-Source Charge	Q_{gs}		-	4.4	6.6	nC
Gate-Drain Charge	Q_{gd}		-	3.8	5.7	nC
Gate Plateau Voltage	$V_{plateau}$		-	-3.1	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -20A, dI/dt = 100A/\mu s,$ $T_J = 25^\circ\text{C}$	-	38	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	25	-	nC
Diode Forward Current	I_S	$T_C = 25^\circ\text{C}$	-	-	-55	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with 10 μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^\circ\text{C}, V_{DD}=-20V, V_{GS}=-10V, L=1.0\text{mH}$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Electrical and Thermal Characteristics

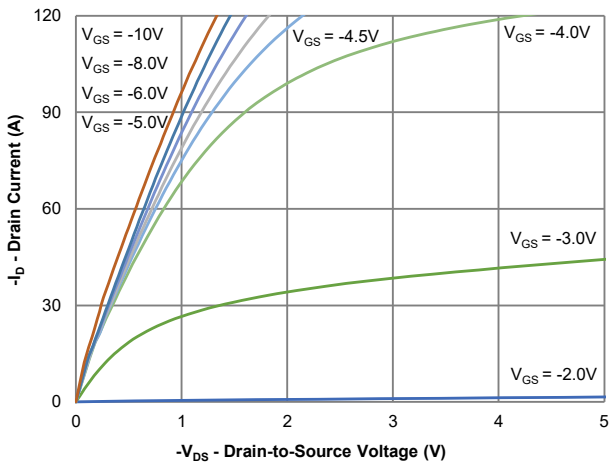


Figure 1: Output Characteristics

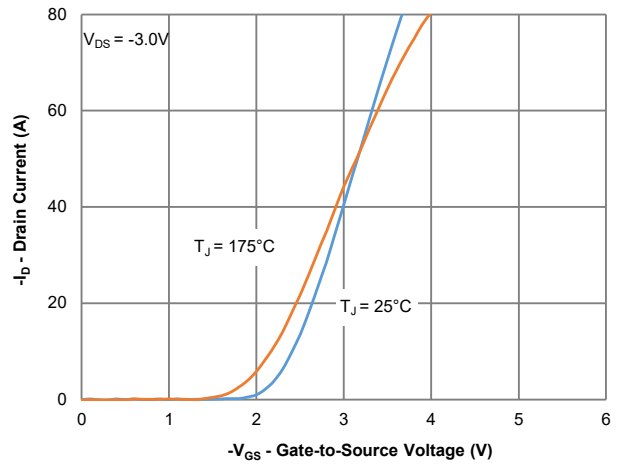


Figure 2: Transfer Characteristics

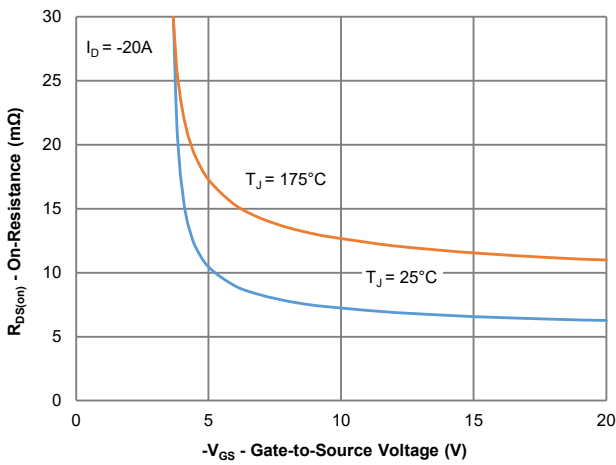


Figure 3: On-Resistance vs. Gate-Source Voltage

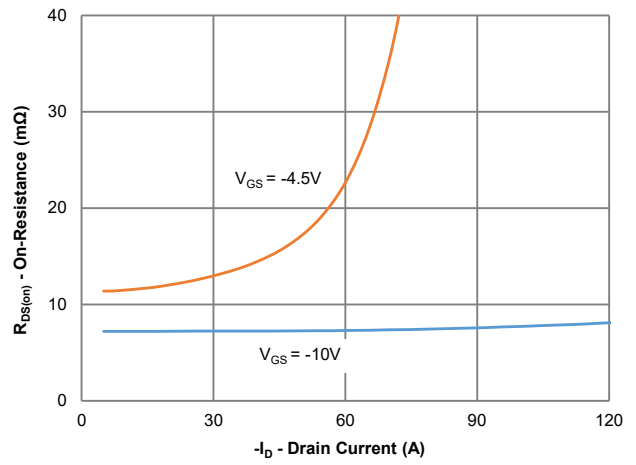


Figure 4: On-Resistance vs. Gate-Source Voltage

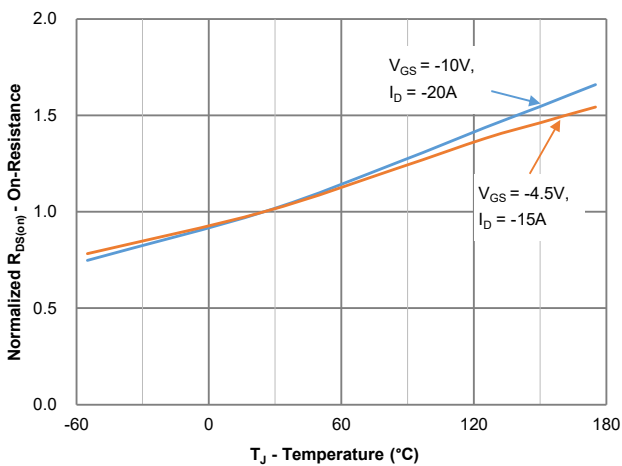


Figure 5: On-Resistance vs. Junction Temperature

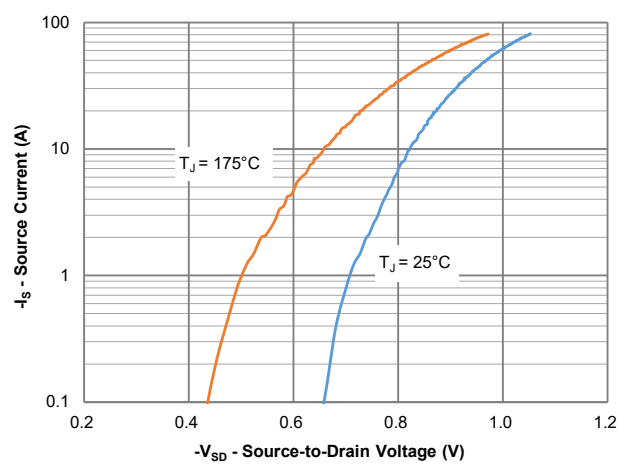


Figure 6: Source-Drain Diode Forward Voltage

Typical Electrical and Thermal Characteristics

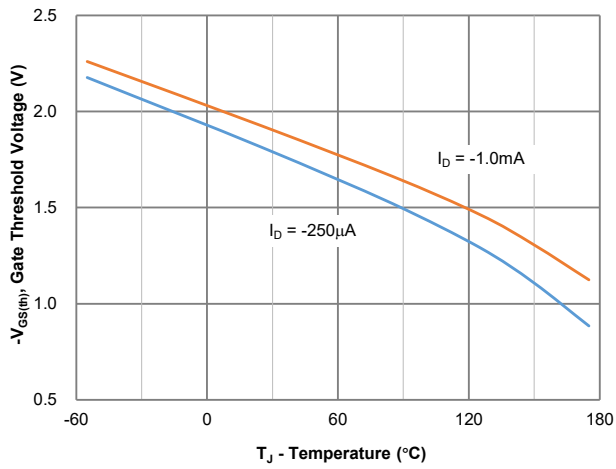


Figure 7: Gate Threshold Variation vs. Junction Temperature

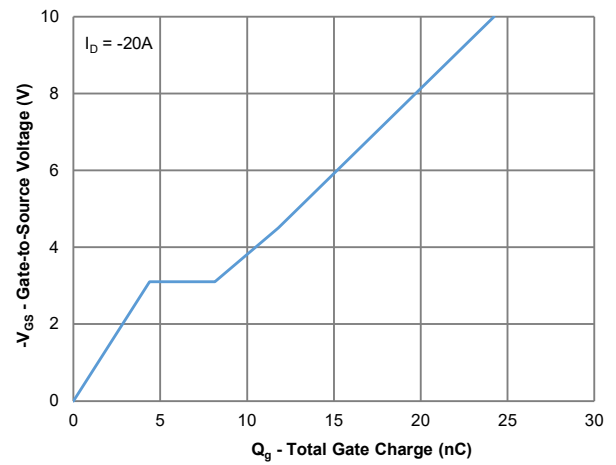


Figure 8: Gate Charge Characteristics

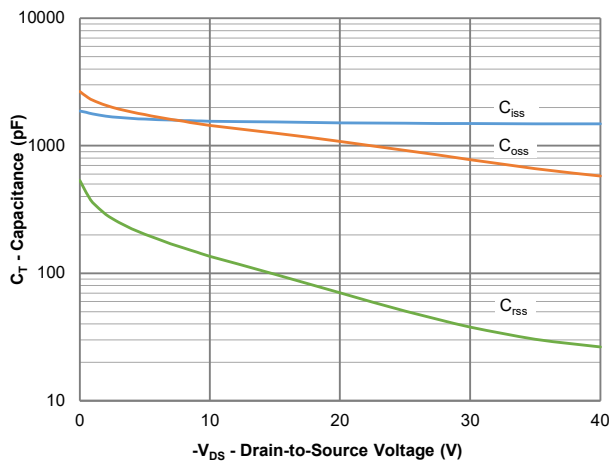


Figure 9: Capacitance Characteristics

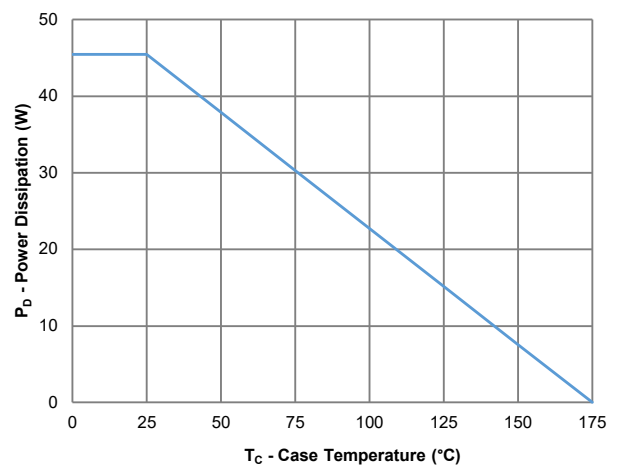


Figure 10: Power Derating

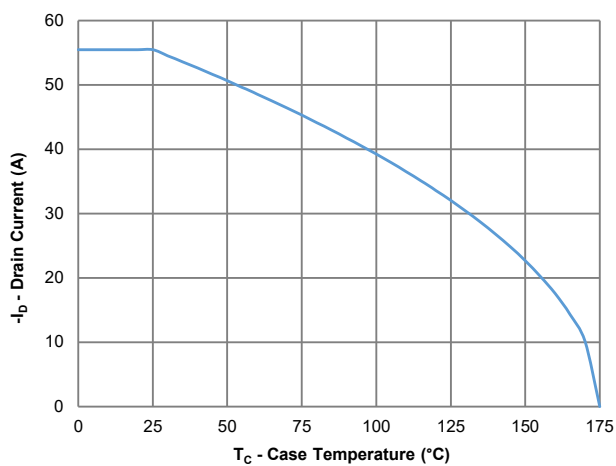


Figure 11: Current Derating

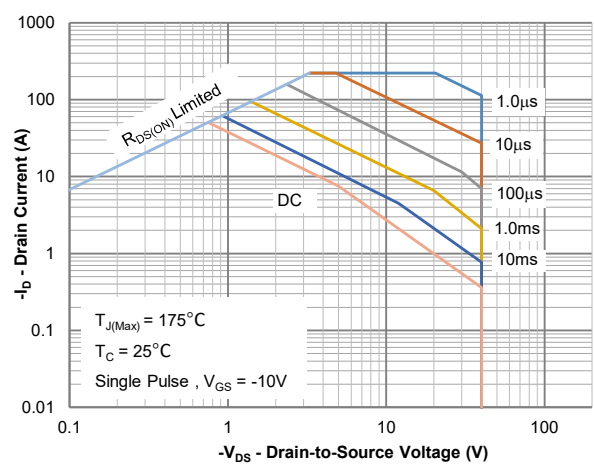


Figure 12: Safe Operating Area

Typical Electrical and Thermal Characteristics

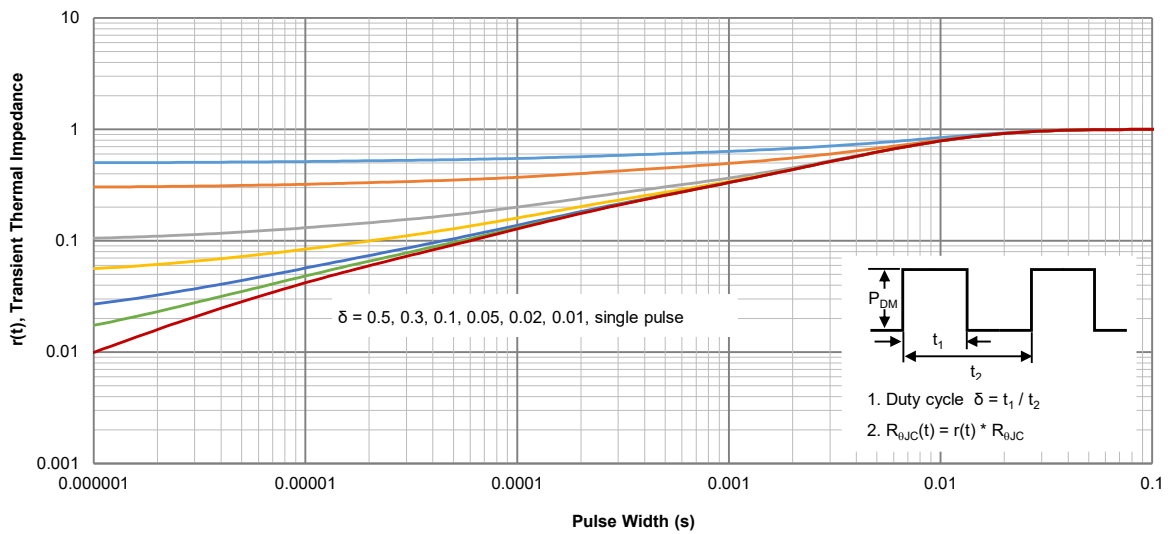
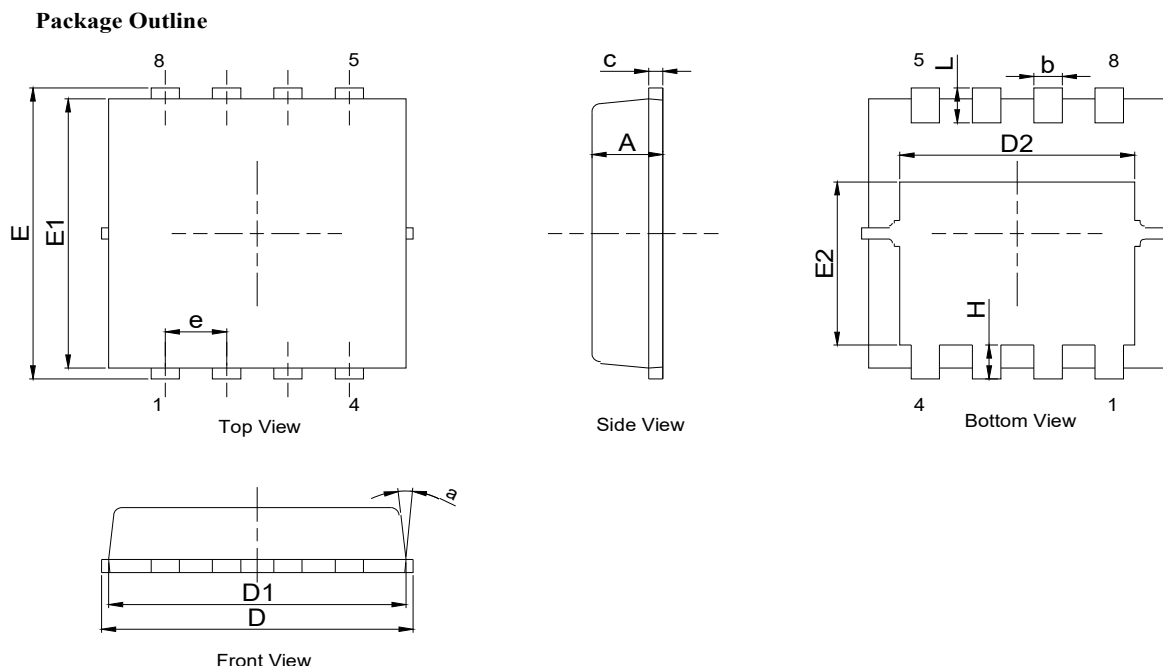


Figure 13: Normalized Maximum Transient Thermal Impedance

PDFN3333-8L Package Outline

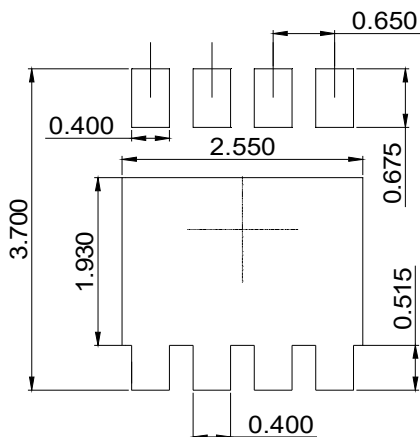


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGL E IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
b	0.20	0.30	0.40
c	0.10	0.15	0.25
D	3.10	3.30	3.40
D1	3.00	3.15	3.25
D2	2.35	--	2.69
E	3.20	3.35	3.45
E1	2.85	3.10	3.20
E2	1.48	--	1.98
e	0.65 BSC		
H	0.25	--	0.60
L	0.25	0.40	0.50
a	---	---	15°

Recommended Soldering Footprint



DIMENSIONS: MILLIMETERS